Pulsed Power Using High-Power Semiconductors

Objectives

This document deals with the application of high-power semiconductors like IGBTs, GTOs, and Thyristors in pulsed power applications.

To achieve the power levels demanded, stacks like the one seen in **Figure 1** enable operating high voltages and high current.

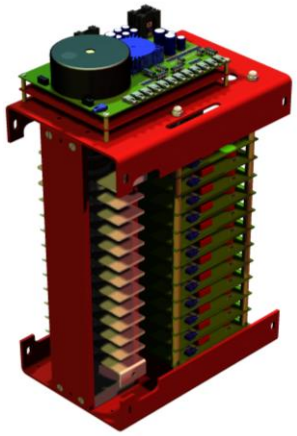

Figure 1: Example of a Stacked Arrangement of High-power Semiconductors

Applications

- Particle physics and research
- Laser drivers
- Ozone generators
- UV-sterilization

Target Audience

This document is intended for engineers interested in or involved with pulsed power applications.

Contact Information

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Introduction

This document is intended to give an overview of the key aspects of the application of high-power semiconductors in pulsed power systems. Consideration is given to the Insulated Gate Bipolar Transistor (IGBT), Gate Turn-Off thyristor (GTO), and conventional thyristor or Silicon Controlled Rectifier (SCR). This application note covers the selection of the appropriate device technology, series and parallel connection of devices, gate drive aspects, and practical implementation.

Power semiconductors have been used in pulsed power systems since the early 1990s in areas such as particle physics and research. More recently, advances in device technology and a greater understanding of device performance under pulse conditions has led to widespread commercial use. In applications such as laser drivers, ozone generators, UV sterilization, and electrostatic precipitators, semiconductor-based switching elements are becoming the norm.

The key drivers for the adoption of semiconductor-based solutions are long term reliability, maintenance free operation, and whole life system costs. The principal obstacles to the adoption of semiconductors are system volume/weight, complexity, and the lack of widely available information. This paper aims to address this last point in particular.

The application and suitability of power semiconductors in pulsed power has been widely reported.[1] to [5]

1. Device Types

There is a wide range of semiconductor devices and technologies available today, many of which have some properties that are attractive for pulsed power applications. However, the two basic groups that perhaps have the most significance to pulsed power are thyristor-based devices and transistor-based devices.

Table 1 gives a brief overview of the more common technologies available today.

Table 1. Overview of Semiconductor Technologies

Thyristor Technologies	Transistor Technologies
Conventional thyristors (SCR) • Symmetric • Asymmetric (fast turn-on) • Distributed gate (fast turn-on) • Reverse conducting	Bipolar Junction Transistors (BJT) • Darlington
Gate Turn-off thyristors (GTO) • Symmetric • Asymmetric • Anode shorted • Transparent emitter • Reverse conducting • Gate commutated (GCT) • Integrated gate commutated (IGCT)	Field Effect Transistors (FET) • Trench • Planar
Other types • MOS Controlled Thyristors (MCT) • Emitter Switched Thyristors (EST)	Insulated Gate Bipolar Transistor (IGBT) • Non-Punch Through (NPT) • Punch Through (PT) • Soft Punch Through (SPT) • Field Stop • Trench

The two thyristor technologies most widely used in pulsed power applications are fast turn-on thyristors and modified gate turn-off thyristors, the latter often referred to as pulse thyristors or fast high current thyristors.

1.1. Fast Turn-on Thyristors

Fast turn-on thyristors achieve their fast switching action by employing either an interdigitated amplifying gate, as seen in **Figure 2**, or by using an asymmetric structure, whereby the reverse blocking capability of the device is sacrificed to optimize the dynamic performance.

(a) Asymmetric Device (b) Distributed Gate Type

Figure 2. Fast Turn-on Thyristor Wafers

Fast turn-on thyristors are available with voltage ratings from sub 1 kV up to around 6 kV and with wafer diameters of up to 100 mm. In general, the physics of semiconductor devices dictates that larger, higher-voltage devices switch slower than lower-voltage, smaller devices. The largest devices can handle pulsed currents of over 100 kA peak and average currents of several thousand amperes can be accommodated with appropriate cooling. The rate of rise of forward current, di_F/dt is often the limiting factor when applying fast turn-on thyristors to pulsed power applications. This is due to the fact that the thyristor is initially triggered around the periphery of the gate structure before the load current then spreads laterally across the wafer. Under high di_F/dt, this can lead to excessively high current density close to the gate structure, which ultimately leads to device destruction.

Modern high-power devices are limited to around 1 kA/µs for repetitive switching and around 2 kA/µs for single shot applications. It is this inherent limitation of di_F/dt capability that has led to the development of modified GTO-thyristor based devices.

1.2. Modified GTO Thyristors or Fast, High-Current Thyristors (FHCT)

Standard GTO thyristors, when operated under conventional conditions, have typical di_F/dt ratings of 300 A/µs to 1000 A/µs. By sacrificing the turn-off capability of the devices, it is possible to achieve and even exceed 20 kA/µs under appropriate conditions. Here too, voltage ratings of up to 6 kV are commercially available and peak current ratings in excess of 140 kA are possible. It is this ability to switch very high voltages and currents at relatively high di_F/dt that has led to the modified GTO thyristor being widely accepted as the component of choice in solid-state pulsed power switch applications. **Figure 3** is an image of a typical GTO thyristor wafer.

Figure 3. GTO Thyristor Wafer

It can be seen that the gate area, visible as yellowish part, actually exceeds the cathode area recognized as the dark fingers. This high level of gate interdigitation gives a standard GTO thyristor its turn-off properties and the modified GTO thyristors their excellent turn-on properties.

Of the commonly available transistor technologies, both FET and IGBT technologies have been used. Large, complex series or parallel arrays of MOSFET transistors have been employed for some applications, particularly where high frequency operation is required. However, by far the most promising devices for pulsed power applications are the latest generation of high voltage IGBTs.

1.3. Insulated Gate Bipolar Transistor (IGBT)

Recent developments in IGBT technology have seen voltage ratings increase from 1.7 kV through 3.3 kV and now up to 6.5 kV. At the same time, newer device structures have facilitated increased current ratings and some characteristics that are potentially attractive for pulsed power applications. Current change rates di_F/dt for IGBTs vary widely between differing technologies and manufacturers, but values between 10 kA/µs and 30 kA/µs have been reported. IGBTs also have the potential for the implementation of turn-off switches. The main drawback of IGBT technology and transistors in general is the relatively limited peak current capability when compared with similarly dimensioned thyristors.

2. Voltage Ratings

Voltage ratings for high power semiconductors must be regarded with respect. Semiconductor devices may be destroyed by over-voltages of as little as 5% lasting for only few microseconds, whereas traditional technologies, such as thyratrons and ignitrons will often survive short over-voltages even if there is some breakdown within the device.

Voltage ratings can be broken down into three basic categories: DC voltage, repetitive peak voltage, and non-repetitive peak or surge voltage. These voltages may or may not be the same for forward and reverse biased conditions. Furthermore, many of these voltage ratings are contingent upon other device conditions such as temperature and gate bias. Care should be taken to read and understand the information given with ratings by manufacturers.

While the peak and surge voltage ratings are self-explanatory, the DC voltage rating is often less clearly defined, if at all. Long term exposure to high DC potentials can reduce the life expectancy of semiconductor devices. **Figure 4** summarizes this relationship for a typical 6.5 kV thyristor with a 100 mm silicon die inside.

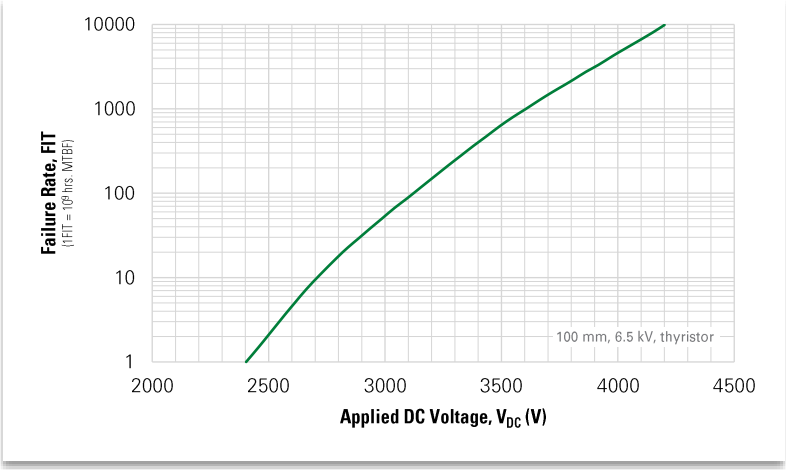


Figure 4. Failure Rate vs. DC-Voltage

For a given failure rate, lower voltage devices can generally operate at a DC voltage closer to their peak rating than higher voltage devices. Smaller diameter devices exhibit lower failure rates at a given DC voltage when compared to large area devices – this is due to the statistical nature of the failure mechanism. Where no rating is given, it is normal to assume 50% of the repetitive peak voltage rating for sufficient long-term reliability of 100 FIT. However, many devices are designed to operate at higher DC potentials. Where this is the case, a specific rating is generally given.

In addition to the so-called static voltage ratings, consideration must be given to dynamic voltages. In particular, many thyristor type devices are sensitive to fast, forward biasing dv/dt ramps. Conventional fast thyristors are available with dv/dt ratings of between 200 V/µs to 1 kV/µs. Modified GTOs are even more sensitive to dv/dt ramps.

Notes on voltage ratings for GTO thyristors:
GTO thyristors, particularly when modified for pulse power applications, require a permanent negative gate bias of typically 2 V or a gate-cathode shunt resistor in order to reliably support the full rated voltage and dv/dt. **Figure 5** and **Figure 6** reveal these relationships, normalized for a typical pulse thyristor.

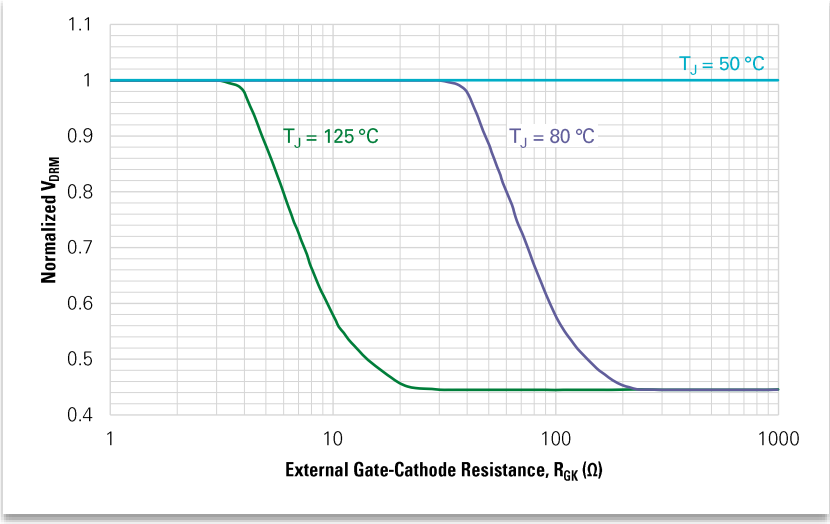


Figure 5. Blocking Voltage vs Gate-cathode Resistance

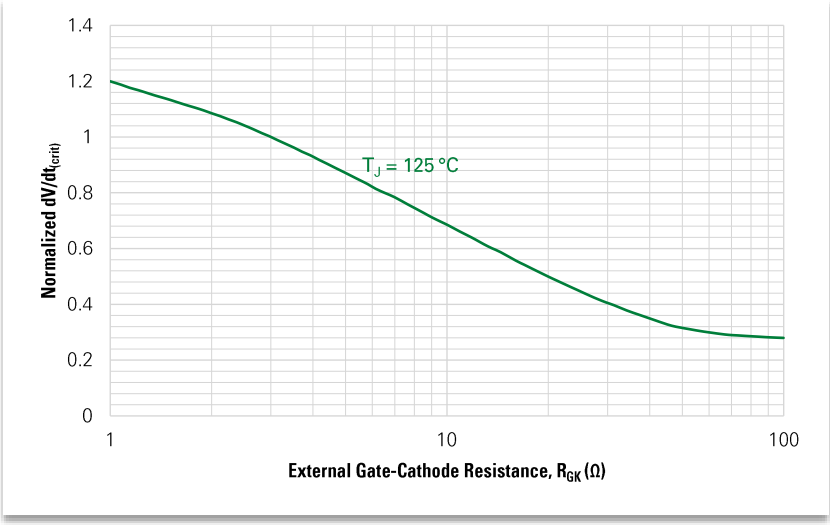


Figure 6. dv/dt vs Gate-cathode Resistance

3. Current Ratings

Average current ratings for power semiconductors are primarily limited by the maximum junction temperature and the thermal impedance of a given device. The peak current rating has additional limitations associated with device physics, design, and technology. There are some distinct differences between thyristor-based devices and transistor-based devices.

3.1. Thyristor-type Devices

The majority of thyristor type devices are based on a four-layer structure and are known as regenerative devices. This means that the more current that flows through the device, the more the conductivity of the silicon is modulated to accommodate current flow. An example of the output characteristic for a modified GTO thyristor is given in **Figure 7**.

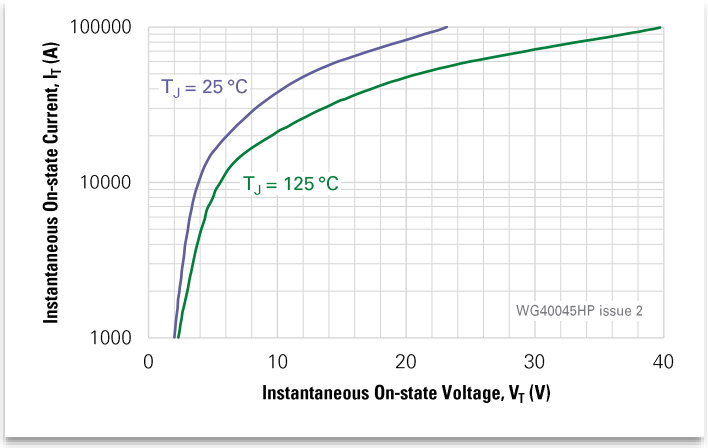


Figure 7. Modified GTO Thyristor Output Characteristic

3.2. Transistor-type Devices

The various transistor type devices are based on a wide range of technologies including bi-polar three layer (n-p-n or p-n-p), various MOS structures and combinations of both as in the IGBT. All transistor devices are, by definition, not regenerative in nature. This means that the conductivity of the device is controlled or at least influenced by the gate voltage or base current. An example of the output characteristic for a high power IGBT is given in **Figure 8**.

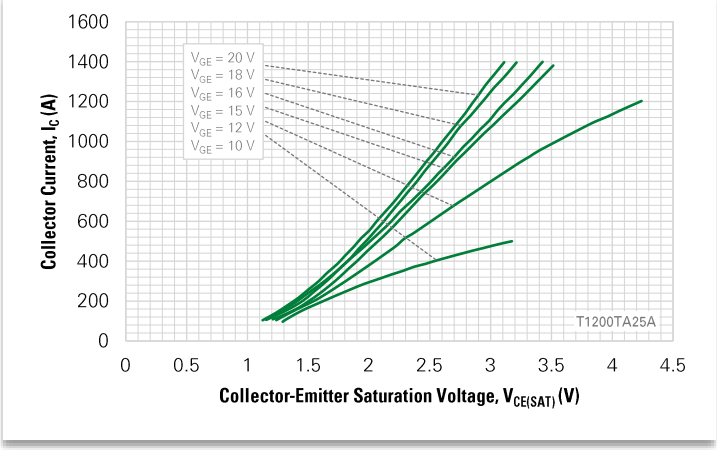


Figure 8. IGBT Output Characteristic

Depending upon the technology employed, most transistor type devices, including IGBTs, exhibit complete saturation at relatively low currents. Indeed, device designers constantly try to control the saturation current to around 4 to 5 times the nominal operating current to facilitate fault current limitation and the ability to safely handle circuits. This is often not desirable for pulsed power applications, where peak current requirements are generally high. It is worth noting, however, that some technologies offer higher peak current ratings. For example, trench gate technology devices often exhibit saturation currents of up to 10 times the nominal operating current for short pulse durations. In general, many high voltage devices have very high peak current capabilities as a side effect of designers trying to reduce conduction losses.

4. Gate Drive Requirements and Switching

The gate drive techniques used to drive power semiconductors can have a marked influence on the dynamic performance of the device. In particular the performance of modified GTO thyristors and IGBTs is highly dependent upon gate drive. Therefore, it deserves special attention.

4.1. Modified GTO Thyristors

All bipolar thyristors, including GTOs, are current controlled devices. In order to achieve fast and efficient switching of any thyristor type device, it is important to provide a strong gate pulse. This is of particular importance for GTO thyristors in pulsed power applications. The value of trigger current for a typical GTO maybe 1 A to 2 A at 25°C. However, it is common to use gate currents of over 200 A with sub microsecond rise times in pulsed power applications. The reasons for this are outlined in **Figure 9**, displaying a typical modified GTO thyristor switching waveform for a 2.5 kV, 66 mm device. The device is switching from 1.5 kV_{DC} into a peak current of over 70 kA.

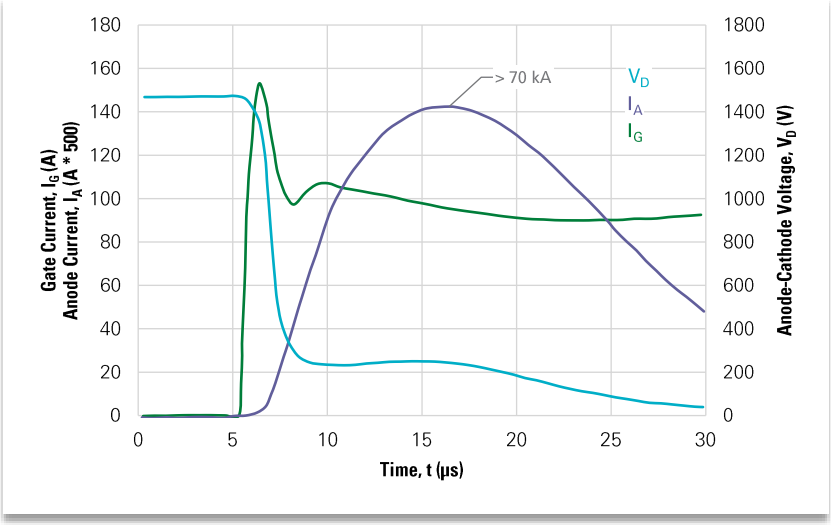


Figure 9. Modified GTO Thyristor Switching Waveforms [2]

A more detailed look to the turn-on process is depicted in **Figure 10**. The gate current waveform can be seen to have a peak value of over 150 A with a rate of rise of 300 A/µs.

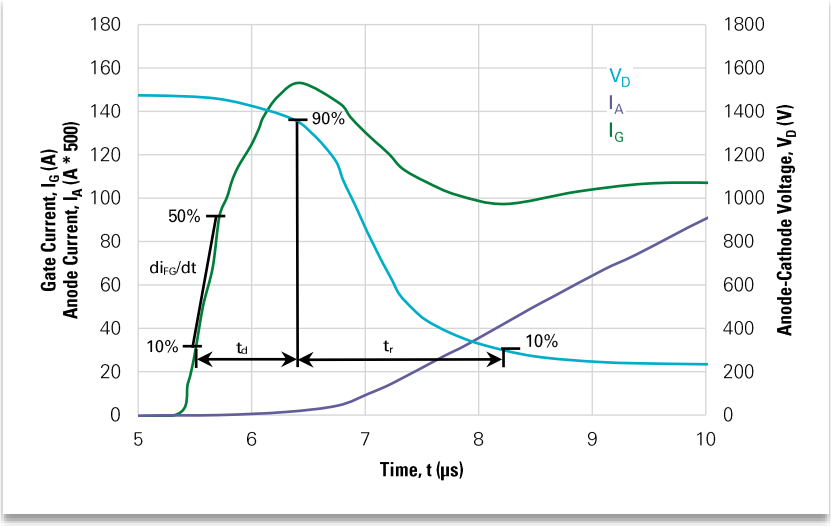


Figure 10. Modified GTO Turn-on, Zoom-in

This combination of high peak gate current I_{GM} and fast rising pulse serves to minimize the inherent device delay time t_d. The high peak gate current also helps to minimize the rise time t_r, measured as the voltage V_D falls. The gate-controlled turn-on time t_{gt} of the device is defined as the sum of t_d and t_r. The effects of peak gate current and rise time are summarized in **Figure 11** and **Figure 12**.

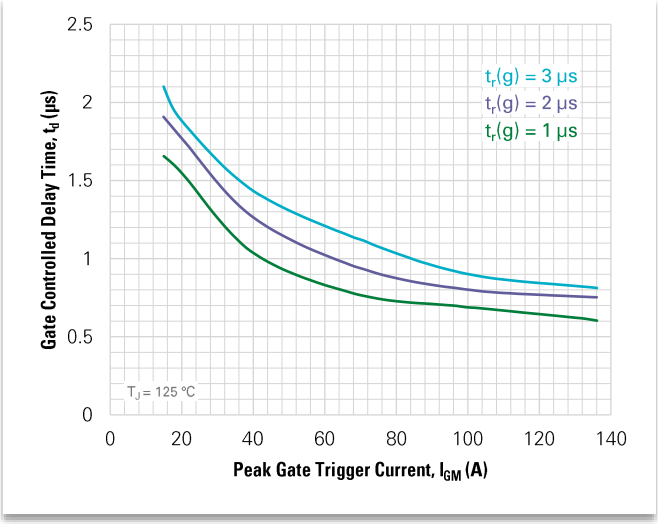


Figure 11. Delay Time t_d vs I_{GM} vs $t_{r(g)}$ [1]

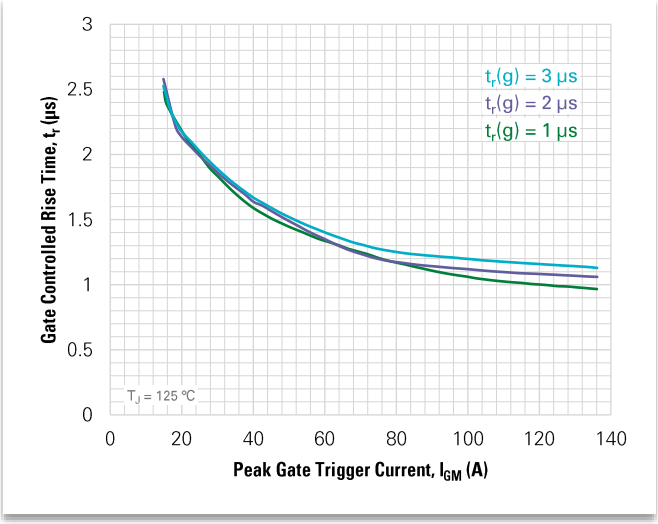


Figure 12. Rise Time t_r vs I_{GM} vs $t_{r(g)}$

Figure 13 includes the characteristics of differing technologies and voltages. All devices are modified 75 mm diameter GTOs optimized for pulsed power applications. Devices included are 4.5 kV Anode Shorted, 2.5 kV Anode Shorted, and 4.5 kV symmetrical.

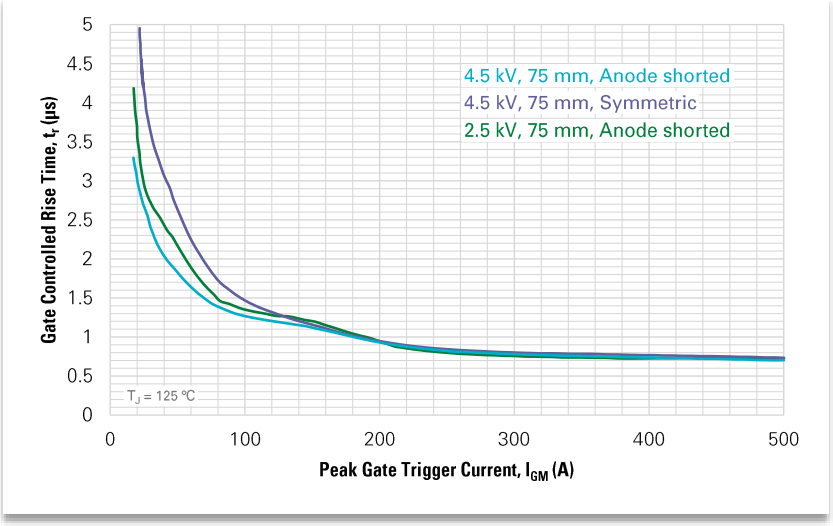


Figure 13. Delay Time t_d vs Peak Gate Current I_{GM} for Different Device Types

4.2. Insulated Gate Bipolar Transistors – IGBTs

IGBTs are MOS-gated devices and, as such, are voltage controlled rather than current controlled. In order to turn on the IGBT as fast as possible, it is necessary to provide a fast-rising gate voltage. At first sight, this may seem to be a simple matter. In fact, the effects of parasitic capacitances within the device make this a little more complicated. **Figure 14** sketches the equivalent circuit for an IGBT including the key parasitic capacitances.

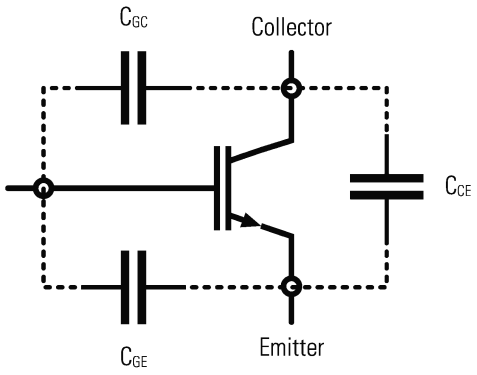


Figure 14. Simplified IGBT-schematic including the Parasitic Capacitances

Turn-on

When a voltage is applied to the gate of the IGBT, the gate-emitter capacitance C_{ge} is charged until the device reaches its threshold voltage and the device begins to switch. As the voltage across the device collapses, a displacement current flows through the gate-collector capacitance C_{gc}, also known as the reverse transfer or Miller capacitance, which opposes the rising gate pulse. To drive the device rapidly, the gate driver must not only charge the gate-emitter capacitance but also provide the displacement current of the gate-collector capacitance. Due to the high change rate of the voltage dv/dt, this current can be quite high, depending on the IGBT's internal set up.

In general, the faster the gate-emitter capacitance is charged, the shorter the delay time remains. The faster the gate-collector capacitance is charged, the faster the rise time of the device and the more efficient the switching action becomes. Most of the commercially available IGBTs contain internal gate resistors in series with the individual silicon chips of between 1Ω and 5 Ω το dampen inter-chip oscillations. This effectively limits the maximum switching speed of the device. Most manufacturers provide comprehensive data of switching times for various external series gate resistors, an example of which is displayed in **Figure 15**. An example of a pulse switching waveform can be seen in **Figure 16**, which details a 160 A / 5.2 kV device switching approximately 1000 A dampened resonant discharge from a 3 kV_{DC} supply.

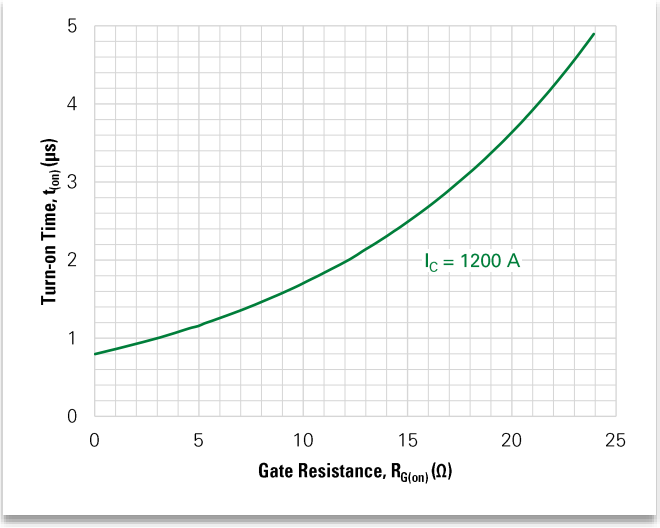


Figure 15. IGBT Turn-on Time vs External Gate Resistor

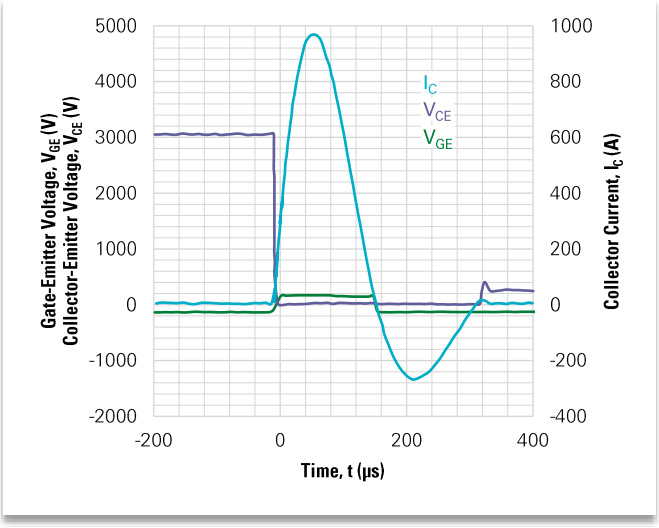


Figure 16. IGBT Pulse Waveforms [3]

Turn-off

Up to this point, only turn-on was considered; however, devices will at some point have to turn-off. The majority of thyristors, with the exception of conventional GTOs, GCTs, and IGCTs, only turn-off when the load current is reduced to zero for a specified period of time. During this time, charge carriers within the semiconductor are removed from the device as it regains its off-state properties. This charge may result in large so-called recovery currents if the device is rapidly reverse biased. There is also another possibility for modified GTOs and some asymmetric thyristors whereby the device is turned off near zero current. This is known as a Gate Assisted Turn-off Thyristor or GATT. This can be very useful for reducing the turn-off time of such devices to practically zero.

In applications where the switch may rapidly be reverse biased, there are some important considerations for the semiconductor. Most thyristor structures will be destroyed by current reversal exceeding 1 kA/µs and therefore a fast series diode may be required for protection. If a reverse conducting switch is required, many asymmetric devices will withstand a reverse avalanche current for several hundred microseconds.

Devices such as IGBTs and IGCTs can be used for hard switching turn-off applications. When designing for turn-off, it is not generally possible to exploit extended current ratings beyond those given in manufacturers' datasheets. As such, the manufacturer's guidelines for a given device should be followed closely.

5. Series Connection

As discussed earlier, device blocking voltage ratings of up to 6.5 kV are commercially available, with +8.5 kV devices in development. To this end, the majority of pulsed power applications require devices to be connected in series. The problems associated with operation arise largely from the inevitable, minor variations in the device characteristics. There are two areas that must be addressed when considering series operation: static voltage balancing and dynamic voltage balancing.

Static Voltage Balancing

In **Figure 17**, the blocking characteristics for three devices T_1, T_2, and T_3 that are considered identical is compared in detail. When connected in series, all devices must carry the same leakage current and, as a result, the voltage will be distributed as denoted by v_1, v_2, and v_3.

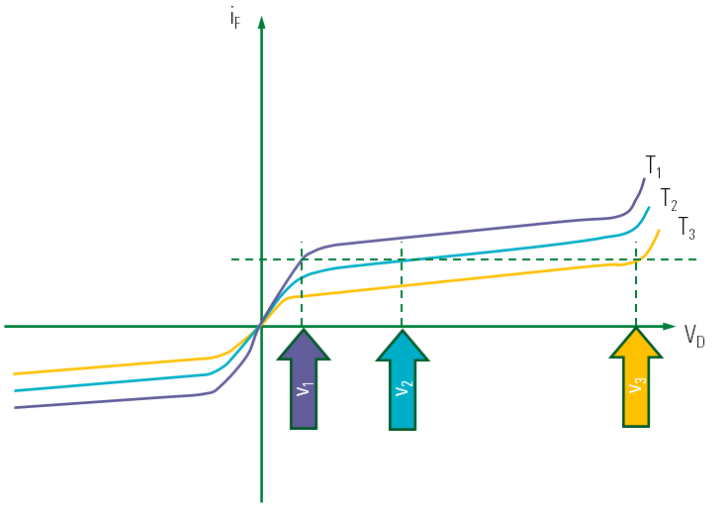


Figure 17. Variations in Off-state Characteristics

This would either lead to an over voltage condition and device failure or necessitate impractical levels of voltage de-rating. There are several practical solutions to this problem, the most common one being the use of voltage sharing resistors connected in parallel with each device. If the resistor current is significantly greater than the device leakage current, then the voltage balancing becomes independent of the individual semiconductor device's characteristics. Worst case conditions when connecting n devices are present with n-1 high leakage devices and 1 low leakage device. In this case, the parallel sharing resistor for each device is approximated by **Equation 1**.

$$R = \frac{n \cdot V_D - V_S}{(n-1)(I_{kx} - I_{kn})} \qquad 1$$

In this equation, V_D is the desired voltage across any device, V_S is the supply voltage the series-connection is connected to while I_{kx} and I_{kn} represent the maximum and minimum device leakage currents.

This can often lead to high power dissipation in the parallel resistors, sometimes in the order of kilowatts. To make a more efficient solution, it is common to match the device characteristics. Further gains are possible by taking maximum device junction temperature and working voltage into account as opposed to device rating. In many applications it is possible to reduce power dissipation in these resistors to less than 10 W per device.

Dynamic Voltage Balancing

There are several aspects to consider under dynamic voltage balancing, including turn-on, turn-off, static dv/dt and reverse recovery where applicable.

Production variations in switching delays can be as much 500 ns under normal operating conditions. Under these circumstances, the last device to turn-on and the first device to turn-off would have to support the entire supply voltage – inevitably leading to device failure. By using very strong gate drive pulses, the delay time for a given device, and moreover the effect of production variations, can be minimized as presented in **Figure 17**, to typically <50 ns. In applications where symmetric devices undergo dynamic reverse biasing, there is a requirement to balance the variations of recovered stored charge – this normally dominates the design criteria. As with static voltage balancing, there are several solutions to the problem, but the most common approach is the use of a capacitance C_S connected across the devices, normally with a series damping resistor R_S. This circuit serves to limit dv/dt from the supply side for a given supply impedance and voltages induced by device recovery whilst also accommodating any variation in switching times. A typical, so-called snubber circuit including static balancing resistors R_P is laid out in **Figure 18**.

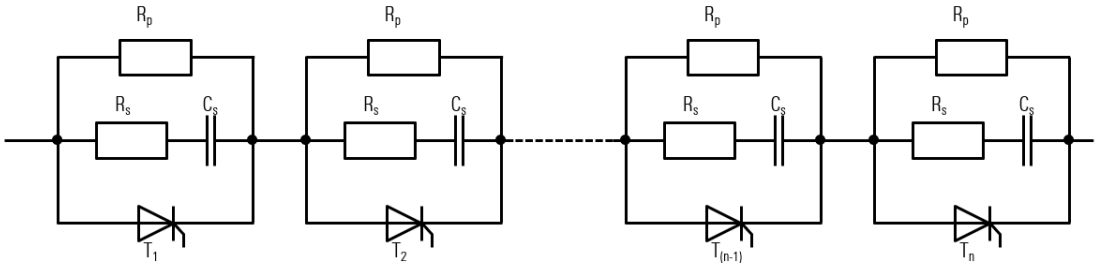


Figure 18. Typical Series-Connection using Snubbers

The approach taken to dimension these components depends to some degree on the application, but some general guidelines are applicable:

Maximum dv/dt

$$dv/dt_{(max)} = 2 \cdot \alpha \cdot \omega_n \cdot V_S = \frac{V_S \cdot R_S}{L} \quad (2)$$

Damping factor

$$\alpha = \frac{R_S}{2 \cdot \sqrt{L/C_S}} \quad (3)$$

Circuit's natural angular frequancy

$$\omega_n = 1/\sqrt{L \cdot C_S} \quad (4)$$

The inductance L in these equations represents the sum of inductances of the overall setup.

It should be noted that with n devices in series, the resulting resistor is $n \cdot R_S$ and the overall capacity is $n^{-1} \cdot C_S$.

In terms of balancing voltage, caused by variations in switching and recovery delays, it is common to equate the difference in delay times to charge. For a given Δt_d and a known switch current waveform, a value for ΔQ can be derived – the integral of the switch current waveform over the period of Δt_d. For turn-off, the same approach can be taken. For reverse recovery, where appropriate device manufacturers will supply and match devices for reverse recovery charge, Q_{rr} again results in a value ΔQ. Once known, it is then a simple matter to calculate the minimum value of snubber capacitor according to **Equation 5**, assuming a maximum transient voltage increase of ΔV.

$$C_S = \frac{\Delta Q}{\Delta V} \quad (5)$$

The peak transient voltage can be up to 80% of the maximum device voltage rating. If the DC voltage rating were 50% of the maximum device voltage rating, then ΔV would be up to 30% of the maximum device voltage rating.

Other Balancing Techniques

There are some alternatives to the balancing circuits described thus far. These involve the use of avalanche devices to limit the voltage across the semiconductor, both in the static and dynamic case. Suitable avalanche devices include metal oxide varistors and avalanche diodes. This approach can be useful when it is undesirable to employ capacitive elements across the switch, for example with negative impedance loads. The application of this approach can be limited in frequency due to the power limitations of commercially available avalanche devices.

6. Parallel Connection

In applications requiring currents beyond those possible with a single device, it may be required that devices are applied in parallel. Under pulsed power conditions, it is not easy to guarantee that current will be shared equally between devices due to variations in device delay times, device output characteristics, and variations in parallel circuit impedance. Even proximity and other magnetic effects can influence current sharing in applications with very short rise times. There are a number of useful techniques that can help with these problems. Firstly, by matching parallel semiconductors for delay times and output characteristics and by using a strong gate pulse, it is possible to minimize the inherent current imbalance due to the semiconductor to less than 10% in most applications. In order to reduce the effects of circuit layout, it is important to produce symmetrical parallel current paths. For example, a single pulse forming inductor could be replaced by a number of inductors placed in the individual parallel circuit paths, much improving current sharing. These inductors could even be coupled. In applications where the limitation is related to average rather than peak current, it is possible to multiplex the switching of several devices to reduce the stress on an individual component.

7. Power Losses

As with all switching devices, power semiconductors exhibit power loss during both conduction and switching.

Conduction Losses

The product of current and voltage given in the output characteristic as shown in **Figure 7** and **Figure 8** may be used to approximate the conduction losses. The output characteristics can be approximated by the linear function in **Equation 6**.

$$V = V_0 + I \cdot r_S \quad \textbf{6}$$

Here, V_o and r_s are the threshold voltage and slope resistance respectively. In this case, the conduction energy losses are given by **Equation 7**.

$$E_{con} = \int I \cdot V_0 + I^2 \cdot r_S \quad \textbf{7}$$

Switching Losses

During turn-on, turn-off, or reverse recovery, there can be a short period whereby there is very high power dissipation within the device due to the coincidence of current and voltage as seen in **Figure 10**. It is not practical to calculate these losses and as such, they must be measured in the individual circuit. Device manufacturers may be able to do this in a cooperative manner.

Employing switching aids may also help to reduce these switching losses. Switching aids are components that reduce the incidence of current and voltage, typically by delaying either the rise of current at turn-on or the rise of voltage at turn-off. Examples of these components include saturable reactor snubber circuits.

Total Losses

The total average losses are given by **Equation 8** – summing up the conduction losses, the turn-on, and the turn-off or recovery losses per cycle and then multiplying this by the switching frequency.

$$P_{AV} = f_{sw} \cdot (E_{con} + E_{ON} + E_{OFF}) \quad \textbf{8}$$

Knowing the ambient temperature T_{amb} and the chain of thermal resistances from junction to the cooling medium R_{th}, the semiconductor's junction temperature can be calculated according to **Equation 9**.

$$T_j = R_{th} \cdot P_{AV} + T_{amb} \quad (9)$$

It is important to consider that the thermal resistance given in device datasheets usually assumes line frequency current waveforms and continuous operation. In most pulsed power applications, the current has a very high peak to average ratio. Under these circumstances, the effective thermal resistance R_{th} needs to be replaced by the transient thermal impedance Z_{th}. Individual measurements in a given setup are highly recommended to determine the thermal development in pulse-power applications. It is within the use-case, that the conditions are not compatible to the ones used for determining the datasheet values.

8. System-level Design

To produce a practical switch assembly, it is necessary to integrate the power semiconductor, gate drive electronics, balancing components, cooling, and mechanical support. It is desirable to produce a "5 terminal switch", those being anode, cathode, control, power supply, and common trigger signal. **Figure 19** illustrates this concept.

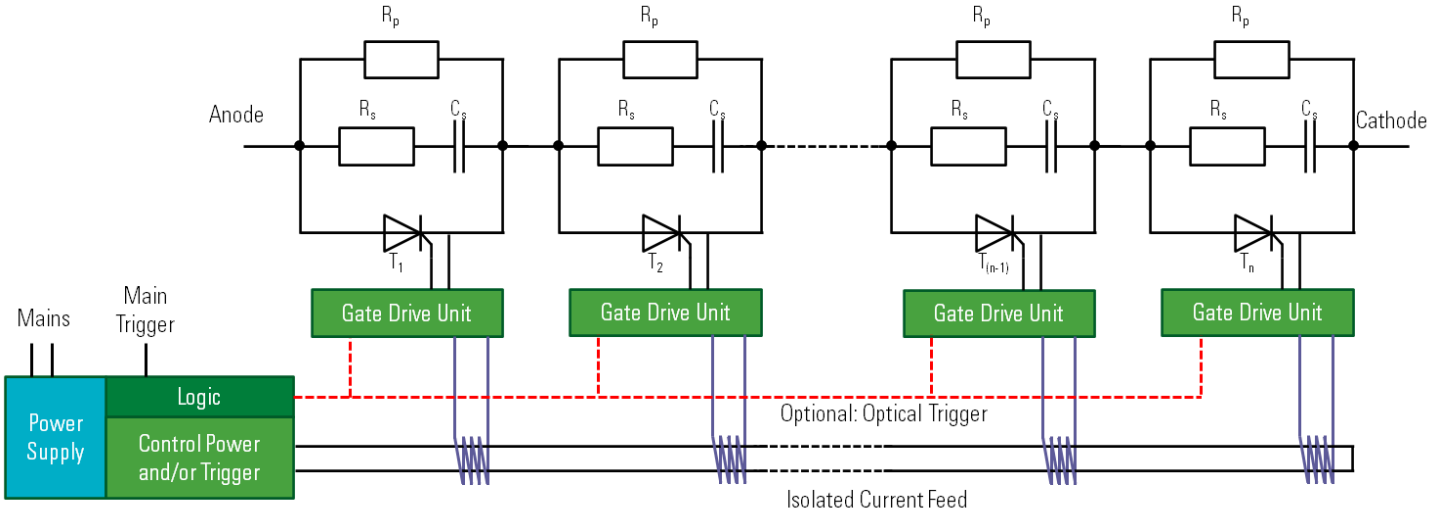
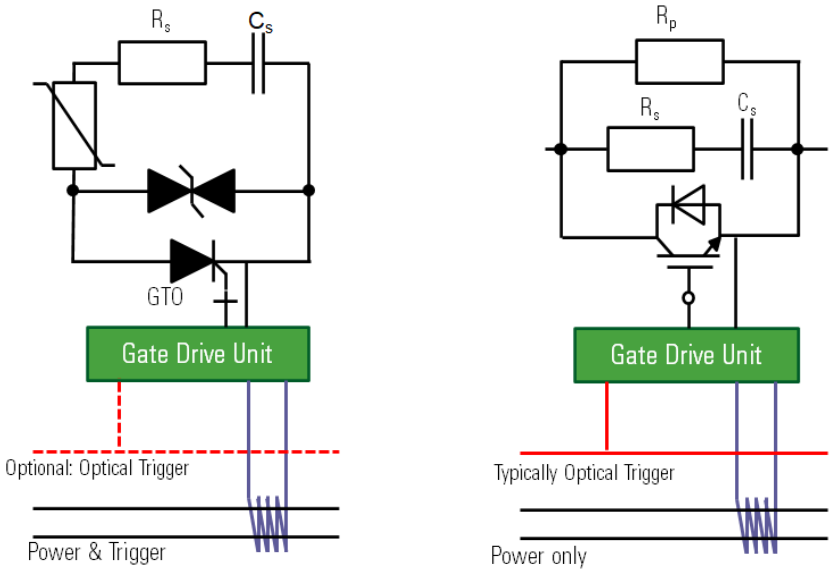


Figure 19. General System Diagram

In this example, there is a master controller which distributes isolated gate power and control signals to the individual switches. Each modular switch consists of a semiconductor, a gate drive unit, and the balancing networks. Some practical examples of these modular switches are given in **Figure 20**, one using a modified GTO thyristor and one using an IGBT.

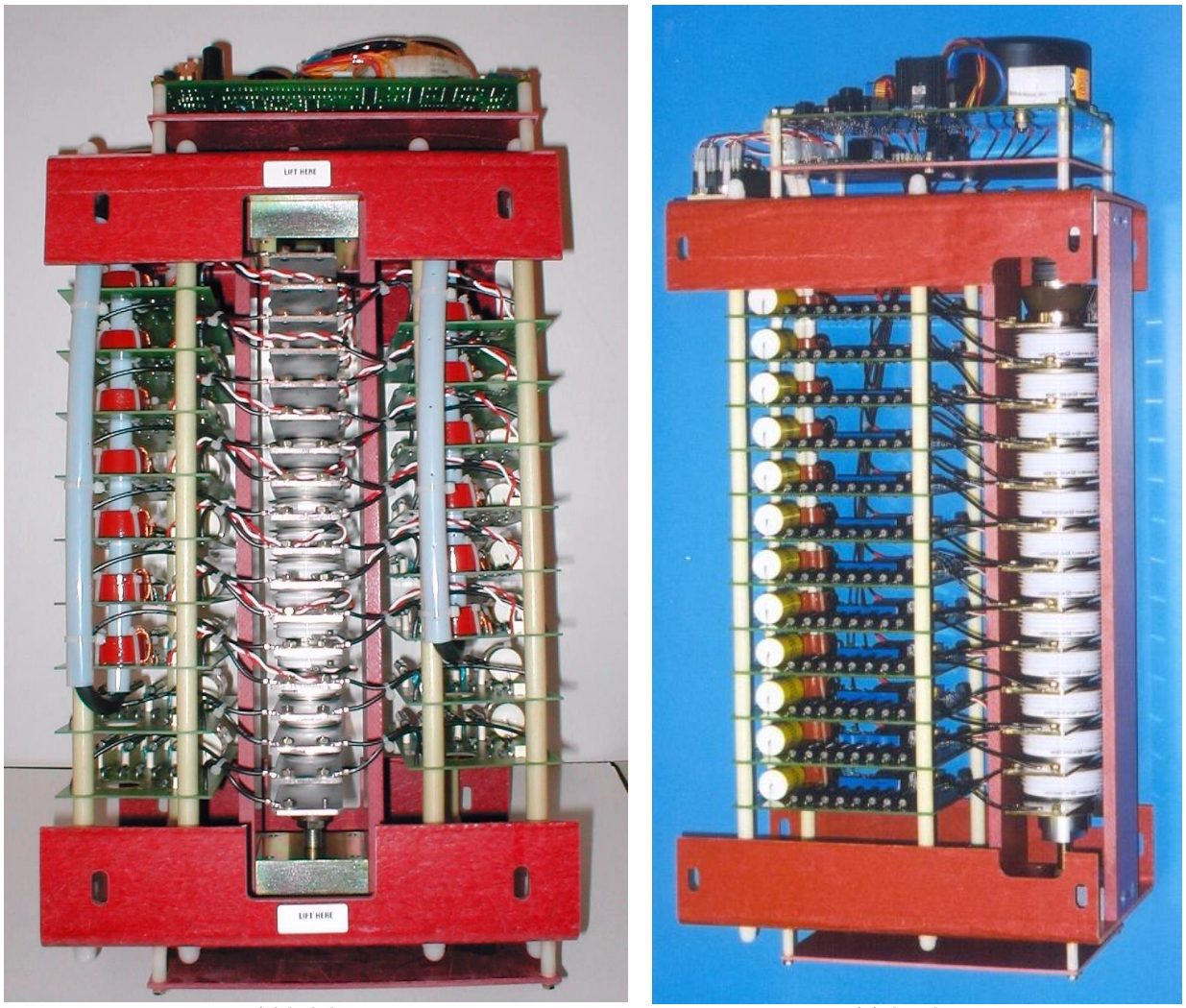


(a) Switch based on Modified GTO (b) Switch based on IGBT and Freewheeling Diode

Figure 20. Examples of Modular Switch Arrangements

Implementation of these examples can be seen in **Figure 21**. The unit depicted in **Figure 21 (a)** comprises of thirteen GTOs, 2.5 kV, 500 A each to achieve a rating of 20 kV_{DC} and is designed to operate at 30 Hz with a 4.5 kA, 20 µs half sine discharge. The GTOs are triggered from a single turn current loop, which is insulated to 40 kV. Current transformers then drive pulse-forming circuits, which provide the gate signals to the GTOs. In this design, silicon-based transient voltage suppressers control static voltage balancing. The R-C snubber circuit is partially decoupled from the load by the use of a varistor.

The unit shown in **Figure 21 (b)** comprises of twelve press-pack IGBTs, 5.2 kV, 160 A each to achieve a rating of 30 kV_{DC} and is designed to operate at 100 Hz with a 1 kA, 150 µs half sine discharge. The unit uses relatively conventional fiber optically triggered gate drives, which are powered from a 25 kHz, 5 A constant current loop. In both cases, a master control unit monitors and controls minimum gate pulse width, maximum frequency, glitch suppression and power supplies – the switch is only permitted to trigger under 'safe' conditions.



(a) GTO-Stack (b) IGBT-Stack

Figure 21. Examples of Integrated Switch Assemblies

9. Summary

Power semiconductor devices, in particular modified GTO thyristors and high voltage IGBTs, can be usefully applied in pulse power applications. The importance of using strong gate drive techniques to exploit extended device ratings has been discussed along with some of the practical application aspects. Integrated, so-called 5 terminal solutions have been proposed.

Most power semiconductor manufacturers are able to offer specific product– and application support for pulsed power and will assist with optimizing an individual solution.

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